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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/903,480	07/11/2001	Takahiro Okada	P/1071-1398	9330

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/903,480	Applicant(s) OKADA ET AL.	
	Examiner Ayal I. Sharon	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *29 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-4 of U.S. Application 09/903,480, originally filed on 07/11/2001 have been presented for examination. The application claims priority to Japanese Application 2000-219075, filed on 07/19/2000.
2. The response filed on 7/29/2005 consists of arguments only. No claims have been amended, cancelled, or added.
3. Examiner finds Applicants' arguments to be unpersuasive. Therefore, this action is final.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
5. The prior art used for these rejections is as follows:
6. Japanese Patent Publication 10-171773. (Henceforth referred to as "**JPO Publication 1**").
7. Japanese Patent Publication 10-242720. (Henceforth referred to as "**JPO Publication 2**").

8. Japanese Office Action issued July 6, 2004. Item No. CA in Applicant's IDS filed on 7/22/2004. (Henceforth referred to as "**JPO Office Action**"). The applicants have provided an English translation of the Abstract of JPO Publication 1, but not for JPO Publication 2. JPO Office Action summarizes the teachings of both references as follows:

The JPO Office Action recites that JPO Publication 1:

> ... describes the fact that the property adjustment of a filter is carried out on the basis of the adjustment knowledge as calculated by using a circuit simulator.

Moreover, the JPO Office Action recites that JPO Publication 2:

> ... describes the fact that, subsequent to obtaining the amount of a change in the resonant frequency as compared with the amount of the change in the structural parameter of a di-electric resonator beforehand by means of a FEM simulator, fine adjustment is actually carried out.

9. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by JPO Publication 2.

10. In regards to Claim 1,

1. A method of adjusting characteristics of an electronic part, comprising:

(a) measuring at least one characteristic of said electronic part;

(b) performing an electromagnetic field simulation to determine the value of said characteristic which is to be obtained when the value of at least one structural parameter of said electronic part is varied from a design value; and

(c) adjusting said structural parameter based on step (b).

The Applicants did not provide an English language translation for JPO Publication 2, however, the JPO Office Action recites that JPO Publication 2 reference teaches the following:

> ... describes the fact that, subsequent to obtaining the amount of a change in the resonant frequency as compared with the amount of the change in the structural parameter of a di-electric resonator beforehand by means of a FEM simulator, fine adjustment is actually carried out.

Examiner finds that the "fine adjustment" corresponds to step (c). This "fine adjustment" inherently also requires step (a), otherwise we do not have a base point to measure the magnitude of the adjustment. The comparison of the measured data to the output of the "FEM simulator" corresponds to step (b).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The prior art used for these rejections is as follows:

13. Japanese Patent Publication 10-171773. (Henceforth referred to as "**JPO Publication 1**").

14. Japanese Patent Publication 10-242720. (Henceforth referred to as "**JPO Publication 2**").

15. Rose, Kenneth. "The Mathematics of Success and Failure". <u>IEEE Circuits and Devices Magazine.</u> Nov. 1991. Vol.7, Issue 3, pp.26-30. (Henceforth referred to as "**Rose**").

16. Van Zant, P. Microchip Fabrication: A Practical Guide to Semiconductor Processing. ISBN 0-07-135636-3. © 2000. Chapter 15. (Henceforth referred to as "**Van Zant**").

17. Japanese Office Action issued July 6, 2004. Item No. CA in Applicant's IDS filed on 7/22/2004. (Henceforth referred to as "**JPO Office Action**"). The applicants have provided an English translation of the Abstract of JPO Publication 1, but not for JPO Publication 2. JPO Office Action summarizes the teachings of both references.

18. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

19. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over JPO Publication 2 in view of Rose.

20. In regards to Claim 2,

> 2. A method of adjusting characteristics of an electronic part, comprising:
>
> (a) measuring at least one characteristic of said electronic part;
>
> (b) performing an electromagnetic field simulation to determine a value of said characteristic which is to be obtained when the value of at least one of a plurality of structural parameter of said electronic part is varied from a design value, said plurality of structural parameters being dimensions of a plurality of pre-selected portions of said electronic part;
>
> (d) adjusting the value of said structural parameter by an amount corresponding to said amount of variation.

The Applicants did not provide an English language translation for JPO Publication 2, however, the JPO Office Action recites that JPO Publication 2 reference teaches the following:

> ... describes the fact that, subsequent to obtaining the amount of a change in the resonant frequency as compared with the amount of the

> change in the structural parameter of a di-electric resonator beforehand by means of a FEM simulator, fine adjustment is actually carried out.

Examiner finds that the "fine adjustment" corresponds to step (d). This "fine adjustment" inherently also requires step (a), otherwise we do not have a base point to measure the magnitude of the adjustment. Examiner also finds that the di-electric resonator structural parameter data output by the "FEM simulator" corresponds to step (b).

However, JPO publication 2 does not teach the following limitation:

(c) determining the amount of validation of the value of the structural parameter
from the design value which has to be effected to make the measured value of said characteristic fall within a predetermined range of allowable error from the design value;
and

Rose, on the other hand, expressly teaches (see p.27, left column, last para. to middle column, 1st para.):

> As SPC is typically practiced, a manufacturing engineer takes a random sample of n chips from a batch of N chips, and determines the number of chips that exceed product tolerances. ...
>
> To answer this question, suppose that the product parameter of interest – threshold voltage, for example – is normally distributed about some mean (μ), say, 1.0 V; and the standard deviation, σ, is 100 mV. For a normal distribution, 95.5 percent of all samples will lie within $\pm 2\sigma$ of the mean; 99.7 percent will lie within $\pm 3\sigma$. If our circuit can only tolerate threshold voltage variations from 0.8 to 1.2 V, almost 5 percent of the circuits would be defective.

Examiner finds that Rose's "product tolerances" correspond to Applicant's "predetermined range of allowable error from the design value."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of JPO publication 2 with those of Rose, because Rose teaches (emphasis added):

> Professor Ishikawa of the University of Tokyo has suggested that quality control evolved in three stages: inspection, manufacturing-process controls, and design improvement. Inspection may prevent bad products from leaving the factory, but it does not reduce product variation. Manufacturing-process controls can reduce production variation, but process corrections are often costly. **Design improvements usually offer the greatest leverage in reducing variation and improving product quality.**
> (see Rose: p.29, left column, 1st para. of "New Strategies for SPC")
>
> **Taguchi formulated an approach to improving product quality at the design stage.** (Ref. 4 provides an excellent introduction to Taguchi's approach.) Once a prototype design is developed, parameter design identifies process settings that reduce product variations. Once these settings are determined, tolerance design determines tolerances that reduce losses over the life of a product.
> (see Rose: p.30, left column, 2nd para.)

21. **Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over JPO Publication 2 in view of Rose and further in view of Van Zant.**

22. In regards to Claim 3,

3. A method of adjusting characteristics of an electronic part according to claim 2, further comprising the steps of:

determining, from the results of said electromagnetic field simulation, correlations between the amounts of validations of the value of the structural parameter and the amounts of deviations of the value of said characteristic from the design value;

and storing the correlations in the form of table data;

wherein the amount of variation of the value of the structural parameter, determined in step (c) and corresponding to the amount of deviation of the measured value of said item of the characteristics from the design characteristic value, is derived from said table data.

Rose teaches:

> As SPC is typically practiced, a manufacturing engineer takes a random sample of n chips from a batch of N chips, and determines the number of chips that exceed product tolerances. ...
>
> To answer this question, suppose that the product parameter of interest – threshold voltage, for example – is normally distributed about some mean

> (μ), say, 1.0 V; and the standard deviation, σ, is 100 mV. For a normal distribution, 95.5 percent of all samples will lie within ± 2σ of the mean; 99.7 percent will lie within ± 3σ. If our circuit can only tolerate threshold voltage variations from 0.8 to 1.2 V, almost 5 percent of the circuits would be defective.
> (see Rose: p.27, left column, last para. to middle column, 1st para.)

However, Rose does not expressly teach "storing the correlations in the form of table data."

Van Zant, on the other hand teaches storing the data in the form of a graph:

> A first step in process control is to make a histogram of the particular process parameter and determine if the distribution is a normal distribution. If it is not, the chances are good that there is something wrong in the process. If the distribution is a normal one, the next step is to compare the range of the distribution with the design limits for the particular parameter (Fig.15.13). This comparison is made to determine if the natural process distribution limits fall within the design limits. If they do not, the process must be fixed or some percentage of the parameter readings (and the wafers) will always be out of specification.
> (see Van Zant: Fig.15.13 and p.490)

Examiner finds that constructing Van Zant's graph inherently requires the storage of the correlations in the form of table data, in order to enable the step of "... compar[ing] the range of distribution with the with the design limits for the particular parameter (Fig.15.13)." Without storing the (X,Y) values of the curve plotted in Fig.15.13, it is not possible to perform the comparison (See Figs. 15.11 to 15.12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Rose with those of Van Zant, because Van Zant's graph is "A first step in process control" (see Van Zant:

p.490, para.2). The Rose reference is also in the field of "statistical process control".

23. In regards to Claim 4,

> 4. A method of adjusting characteristics of an electronic part according to claim 3, wherein steps (a)-(d) are cyclically repeated while setting the amount of adjustment in step (d) in each cycle to a value smaller than said amount of variation, thereby bringing the value of said characteristic closer to the design value.

Rose expressly teaches (emphasis added):

> **Continuous quality improvements are not optional** if one wishes to remain competitive in microelectronics manufacturing. The unprecedented rate of improvement in microelectronics technology requires **very rapid improvement in process quality**. Knowing the techniques of statistical process control is essential for maintaining and improving process quality. This is especially true at the stage of product and process development where SPC techniques offer the greatest leverage. **Continuing reductions in the sensitivities of product parameters to process variations will assure continuous quality improvement.** In addition, defect densities must be reduced significantly as design rules shrink to avoid catastrophic failures and assure reasonable yields.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Rose with those of Van Zant, because Van Zant's graph is "A first step in process control" (see Van Zant: p.490, para.2). The Rose reference is also in the field of "statistical process control".

Response to Arguments

24. Applicant's arguments filed 7/29/2005 have been fully considered but they are not persuasive.

25. In regards to claims 1 and 2, Applicants have unpersuasively argued the following (see arguments filed 7/29/2005, p.6):

> [The prior art reference] JP10-242720 does not teach or suggest performing an electromagnetic field simulation to determine a value of the characteristic which is to be obtained when the value of at least one structural parameter of the electronic part is varied from a design value, as required by independent claims 1 and 2."

26. Examiner refers the Applicants to paragraphs [0019] and [0020] of the English language translation of JP10-242720, which the Applicants provided along with the arguments filed 7/29/2005.

27. Paragraph [0019] of the English language translation of JP10-242720 reference teaches:

> [I]t is the result of calculating the variation of the resonance frequency when changing h, and the resonance frequency to the variation of h by FEM simulation.

Paragraph [0020] of the English language translation of JP10-242720 reference teaches:

> Moreover, h=9.0-8.5[mm]. The variation of resonance frequency to the variation which it is at the time h serves as max, and it is 52.4[MHz/mm]. ... Thus by [of a dielectric plate] adjusting the depth of a hole 6 near a center mostly, resonance frequency can be changed a lot and resonance frequency can be finely tuned by avoiding the central part of a dielectric plate conversely and adjusting the depth for a hole 6.

28. Examiner finds that the '720 reference's "FEM simulation" corresponds to the claimed "electromagnetic field simulation." The '720 reference's "resonance frequency" corresponds to the claimed "value of a characteristic obtained", and the '720 reference's "depth of a hole 6" corresponds to the claimed "structural parameter of the electronic part varied from a design value."

29. Examiner also notes that the use of FEM simulation as a form of "electromagnetic simulation" in the design of dielectric filters is old and well known. Examiner refers the Applicants to the Maxwell's equations on p.926 of the Cousty et al. reference, "Finite Elements for Microwave Device Simulation: Application to Microwave Dielectric Resonator Filters." (1992).

30. In regards to dependent claims 3 and 4, the Applicants argue that they depend from dependent claim 2. Applicants also argue (see arguments filed 7/29/2005, p.6):

> Each of these dependent claims include additional limitations which, in combination with the limitations of the claims from which they depend, are neither disclosed nor suggested in the art of record.

31. Applicants' argument regarding claims 3 and 4 is not persuasive because it does not address the detailed rejections presented in the previous Office Action. Examiner does not find this one sentence assertion to be persuasive, and is maintaining the rejections.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

33. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

35. Cousty et al. “Finite Elements for Microwave Device Simulation: Application to Microwave Dielectric Resonator Filters.” <u>IEEE Transactions on Microwave Theory and Techniques.</u> May, 1992. Vol.40, Issue 5, pp.925-932. (Teaches that FEM simulation is a form of “electromagnetic simulation” in the design of dielectric filters. See especially Maxwell’s equations on p.926).

36. Lee, Moon-Que et al. “Efficient Coupling Patterns Design of Miniaturized Dielectric Filter Using EM Simulator and EPO Technique.” <u>IEEE MTT-S International Microwave Symposium Digest.</u> June, 1996. Vol.2, pp.737-740. (Teaches an Optimization algorithm for iteratively changing structural component values in order to adjust the value of a characteristic obtained. See Figs. 3-5 and Table 1).

37. Bandler, J.W. et al. “Design Optimization of Interdigital Filters Using Aggressive Space Mapping and Decomopsition.” <u>IEEE Transactions on Microwave Theory and Techniques</u>. May 1997, Vol.45, Issue 5, pp.761-769. (Builds on the iterative

'course' and 'fine' model technique taught in Lee. See Table 1 for a table that stores parameters).

38. Kang, C.Y. et al. "Computer-Aided Design of Monoblock Dielectric Filter for PCS." 1999 Asia Pacific Microwave Conference. Nov. 1999. Vol.2, pp.291-294. (Uses FEM models to solve for electro-magnetic parameters, especially the last paragraph of p.292).
39. Sun, Jwo-Shiun et al. "Simulations of the Microwave Dielectric Filters." 2001 Asia-Pacific Microwave Conference. Dec. 2001. Vol.3, pp.1016-1019. (Uses FEM to simulate EMF in dielectric filters. This reference pre-dates the U.S. filing date of the instant application, but post-dates the priority filing date of this application).
40. Yao, H.-W. et al. "Analysis of Quarter Wavelength Ceramic Combline Filters." IEEE MTT-S International Microwave Symposium Digest. June 1996. Vol.2, pp.473-476. (Teaches Resonant Frequency as a function of structural component parameters.)
41. Yao, H.-W. et al. "Quarter Wavelength Ceramic Combline Filters." IEEE Transactions on Microwave Theory and Techniques. Dec. 1996. Vol.44, Issue 12. pp.2673-2679. (Teaches Resonant Frequency as a function of structural component parameters.)
42. U.S. Patent 5,576,674 to Jachowski. See col.16, line 60 to col.17, line 19. Teaches the tuning of dielectric filters by using as imulator.
43. JP 09-312509. Teaches the use of simulation to adjust a structural component value in a dielectric filter.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

October 12, 2005

Paul L. Rodriguez 10/13/05

Primary Examiner
Art Unit 2125